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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,646	02/05/2001	Susumu Takahashi	202447US2	8312
22850	7590	03/13/2008		
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				
EXAMINER				
SINGH, RACHNA				
ART UNIT		PAPER NUMBER		
2176				
NOTIFICATION DATE		DELIVERY MODE		
03/13/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

09/775,646

Applicant(s)

TAKAHASHI ET AL.

Examiner

Rachna Singh

Art Unit

2176

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 65-91 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 65-91 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
- Paper No(s)/Mail Date: _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This action is responsive to communications: Amendments and Remarks filed on 12/20/07.
2. Claims 65-91 are pending. Claims 65, 73, 80, and 87 are independent claims which have been amended.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 65-66, 73-74, 80-81, and 87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamaki et al., US 2001/0014836 A1, 8/16/01 (filed 2/12/01, continuation filed 6/19/98).

Regarding Independent Claims 65, 73, 80, and 87, Tamaki discloses a production planning system in which a production plan comprises a data storage unit for storing parts list information providing a list of required parts, a parts stock storage

section indicating parts stock information which meets the preamble, **a system for creating and/or editing structured parts**. See abstract and page 6, paragraphs [0117]-[0118]. Tamaki discloses a unit for storing production plan information on how to produce a particular product such as an electronic circuit board along with a parts list storage section for storing the parts list information providing a list of required parts which meets the limitation, **an assembly information storage configured to store assembly information for a plurality of electronic circuit boards, including a name of each electronic circuit board, and storing for each respective electronic circuit board a plurality of parts information including a name of parts utilized in said respective electronic circuit board**. See page 3, paragraph [0033], page 6, paragraph [0118], page 7, paragraph [0127]-[0128] and figures 1 and 3. Tamaki discloses that an electronic circuit board could be one of the products being created on a production line which meets the limitation, **an electronic circuit board**. See page 10, paragraph [0155].

Examiner Note: A "product" is being interpreted as an "assembly". Furthermore, Examiner is interpreting "a list of parts information" as including the name of the parts used in the product.

Tamaki discloses a parts list storage section for storing the parts list information providing a list of required parts for a product which meets the limitation, **a parts information storage configured to store a plurality of said parts information, and parts attribute information including functions of parts corresponding to said parts information**. See page 6, paragraph [0118].

Tamaki discloses retrieving parts information from the production planning information and the parts list information stored in the data storage unit for use in a material resource planning unit. Tamaki discloses that an electronic circuit board could be one of the products being created on a production line which meets the limitation, ***an electronic circuit board***. See page 10, paragraph [0155]. This meets the limitation, ***a parts information retrieving device configured to receive an input of assembly information indicating one of said electronic circuit boards, retrieve a plurality of parts information from said assembly information storage identifying the parts utilized in said indicated electronic circuit board based on the input assembly information, to retrieve the parts attribute information from said parts information storage based on the retrieved parts information, and to retrieve other parts information from said parts information storage based on the retrieved parts attribute information.***

Tamaki discloses an adjusting means in which superfluous or deficient parts are identified from the parts stock information and parts information. Superfluous parts are eliminated as are deficient parts and the production planning system is adjusted accordingly. See page 6, paragraph [0117]-[0122] and page 18. The parts list information is generated by the material resource plan unit for calculating the required amount of material resources based on this list. The production system receives production planning information including parts list information from the parts acquisition system. See page 6. The updated structural parts list is provided to the production planning system where it is stored in a data storage unit which meets the limitation, ***an***

assembly information update device configured to replace the parts information corresponding to the assembly information with other parts information retrieved from the parts information storage, and to store the replaced parts information corresponding to the assembly information in a memory. See page 18, second column.

Tamaki does not expressly teach the “parts attribute information including functions of parts”; however, it was well known in the art at the time of the invention that any part of an assembly has a function. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention that a list of “required parts” would include the function of such parts because a “required part” would be identified by its use or function in the product.

In reference to claims 66, 74, and 81, Tamaki teaches that the parts information in storage may include information regarding a name of the part, a feature such as quantity consumed, a cost evaluation module, etc. See figures 24-27.

5. Claims 67-72, 75-79, 82-86, and 88-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamaki et al., US 2001/0014836 A1, 8/16/01 (filed 2/12/01, continuation filed 6/19/98) in view of Tegethoff, US 5,539,652, 7/23/96.

In reference to claim 67, Tamaki does not teach a compatibility prediction information output device configured to survey on predetermined items (i.e. packaging density, arrangement, and operation verification) based on parts information list created by parts information list creating/editing device and to create and output decision information for compatibility prediction based on results from said survey.

Tegethoff, however, teaches a method for manufacturing test simulation in electronic circuit design. Tegethoff teaches a test simulator that simulates a manufacturing test of boards and multichip modules from design concept to aid the designer in selecting trade-offs in design. The methods models fault probabilities for the circuit design based on the components. Tegethoff further discloses the Manufacturing Test Simulator (MTSIM) which is a concurrent engineering simulation tool for manufacturing test, that is, a tool to predict manufacturing test behavior while a product is still being designed. See column 6. MTSIM uses pareto analysis in which a user can evaluate simulation results to determine faults, test coverage, etc. Pareto analysis can be done at three levels of abstraction including individual components, groups of components with the same part number, and groups of components. All part numbers are assigned a category based on level of integration and functionality. See column 11. Furthermore, Tegethoff teaches that the technology of circuit board assembly is evolving to support density demands of many modern circuit designs. Multi-chip modules and twelve-mil pitch surface mount technology (SMT) are frequently used to improve circuit density. SMT chip packages with lead counts of over 1000 are not uncommon. New fabrication processes are used to enable higher circuit densities usually have higher

defect rates than older low density fabrication technologies. Tegethoff teaches identifying defects in packaging densities. See columns 1-4.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate Tegethoff's prediction concerning operation, simulation, etc in a system of Tamaki's structured parts list because early prediction of manufacturing behavior drives design changes which optimize the product's manufacturability and testability, thus improving product quality and reducing cost and utilizing a parts list would help facilitate this prediction. See column 6 of Tegethoff.

In reference to claim 68, Tamaki does not teach a compatibility prediction information output device configured to survey on predetermined items (i.e. packaging density, arrangement, and operation verification) based on parts information list created by parts information list creating/editing device and to create and output decision information for compatibility prediction based on results from said survey.

Tegethoff, however, teaches a method for manufacturing test simulation in electronic circuit design. Tegethoff teaches a test simulator that simulates a manufacturing test of boards and multichip modules from design concept to aid the designer in selecting trade-offs in design. The methods models fault probabilities for the circuit design based on the components. Tegethoff further discloses the Manufacturing Test Simulator (MTSIM) which is a concurrent engineering simulation tool for manufacturing test, that is, a tool to predict manufacturing test behavior while a product is still being designed. See column 6. MTSIM uses pareto analysis in which a user can

evaluate simulation results to determine faults, test coverage, etc. Pareto analysis can be done at three levels of abstraction including individual components, groups of components with the same part number, and groups of components. All part numbers are assigned a category based on level of integration and functionality. See column 11. Furthermore, Tegethoff teaches that the technology of circuit board assembly is evolving to support density demands of many modern circuit designs. Multi-chip modules and twelve-mil pitch surface mount technology (SMT) are frequently used to improve circuit density. SMT chip packages with lead counts of over 1000 are not uncommon. New fabrication processes are used to enable higher circuit densities usually have higher defect rates than older low density fabrication technologies. Tegethoff teaches identifying defects in packaging densities. See columns 1-4.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate Tegethoff's prediction concerning operation, simulation, etc in a system of Tamaki's structured parts list because early prediction of manufacturing behavior drives design changes which optimize the product's manufacturability and testability, thus improving product quality and reducing cost and utilizing a parts list would help facilitate this prediction. See column 6 of Tegethoff.

In reference to claim 69, Tamaki does not teach a compatibility prediction information output device configured to survey on predetermined items (i.e. packaging density, arrangement, and operation verification) based on parts information list created

by parts information list creating/editing device and to create and output decision information for compatibility prediction based on results from said survey.

Tegethoff, however, teaches a method for manufacturing test simulation in electronic circuit design. Tegethoff teaches a test simulator that simulates a manufacturing test of boards and multichip modules from design concept to aid the designer in selecting trade-offs in design. The methods models fault probabilities for the circuit design based on the components. Tegethoff further discloses the Manufacturing Test Simulator (MTSIM) which is a concurrent engineering simulation tool for manufacturing test, that is, a tool to predict manufacturing test behavior while a product is still being designed. See column 6. MTSIM uses pareto analysis in which a user can evaluate simulation results to determine faults, test coverage, etc. Pareto analysis can be done at three levels of abstraction including individual components, groups of components with the same part number, and groups of components. All part numbers are assigned a category based on level of integration and functionality. See column 11. Furthermore, Tegethoff teaches that the technology of circuit board assembly is evolving to support density demands of many modern circuit designs. Multi-chip modules and twelve-mil pitch surface mount technology (SMT) are frequently used to improve circuit density. SMT chip packages with lead counts of over 1000 are not uncommon. New fabrication processes are used to enable higher circuit densities usually have higher defect rates than older low density fabrication technologies. Tegethoff teaches identifying defects in packaging densities. See columns 1-4.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate Tegethoff's prediction concerning operation, simulation, etc in a system of Tamaki's structured parts list because early prediction of manufacturing behavior drives design changes which optimize the product's manufacturability and testability, thus improving product quality and reducing cost and utilizing a parts list would help facilitate this prediction. See column 6 of Tegethoff.

In reference to claim 70, Tamaki does not teach a compatibility prediction information output device configured to survey on predetermined items (i.e. packaging density, arrangement, and operation verification) based on parts information list created by parts information list creating/editing device and to create and output decision information for compatibility prediction based on results from said survey.

Tegethoff, however, teaches a method for manufacturing test simulation in electronic circuit design. Tegethoff teaches a test simulator that simulates a manufacturing test of boards and multichip modules from design concept to aid the designer in selecting trade-offs in design. The methods models fault probabilities for the circuit design based on the components. Tegethoff further discloses the Manufacturing Test Simulator (MTSIM) which is a concurrent engineering simulation tool for manufacturing test, that is, a tool to predict manufacturing test behavior while a product is still being designed. See column 6. MTSIM uses pareto analysis in which a user can evaluate simulation results to determine faults, test coverage, etc. Pareto analysis can be done at three levels of abstraction including individual components, groups of

components with the same part number, and groups of components. All part numbers are assigned a category based on level of integration and functionality. See column 11. Furthermore, Tegethoff teaches that the technology of circuit board assembly is evolving to support density demands of many modern circuit designs. Multi-chip modules and twelve-mil pitch surface mount technology (SMT) are frequently used to improve circuit density. SMT chip packages with lead counts of over 1000 are not uncommon. New fabrication processes are used to enable higher circuit densities usually have higher defect rates than older low density fabrication technologies. Tegethoff teaches identifying defects in packaging densities. See columns 1-4.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate Tegethoff's prediction concerning operation, simulation, etc in a system of Tamaki's structured parts list because early prediction of manufacturing behavior drives design changes which optimize the product's manufacturability and testability, thus improving product quality and reducing cost and utilizing a parts list would help facilitate this prediction. See column 6 of Tegethoff.

In reference to claim 71, Tamaki does not teach a compatibility prediction information output device configured to survey on predetermined items (i.e. packaging density, arrangement, and operation verification) based on parts information list created by parts information list creating/editing device and to create and output decision information for compatibility prediction based on results from said survey.

Tegethoff, however, teaches a method for manufacturing test simulation in electronic circuit design. Tegethoff teaches a test simulator that simulates a manufacturing test of boards and multichip modules from design concept to aid the designer in selecting trade-offs in design. The method models fault probabilities for the circuit design based on the components. Tegethoff further discloses the Manufacturing Test Simulator (MTSIM) which is a concurrent engineering simulation tool for manufacturing test, that is, a tool to predict manufacturing test behavior while a product is still being designed. See column 6. MTSIM uses pareto analysis in which a user can evaluate simulation results to determine faults, test coverage, etc. Pareto analysis can be done at three levels of abstraction including individual components, groups of components with the same part number, and groups of components. All part numbers are assigned a category based on level of integration and functionality. See column 11. Furthermore, Tegethoff teaches that the technology of circuit board assembly is evolving to support density demands of many modern circuit designs. Multi-chip modules and twelve-mil pitch surface mount technology (SMT) are frequently used to improve circuit density. SMT chip packages with lead counts of over 1000 are not uncommon. New fabrication processes are used to enable higher circuit densities usually have higher defect rates than older low density fabrication technologies. Tegethoff teaches identifying defects in packaging densities. See columns 1-4.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate Tegethoff's prediction concerning operation, simulation, etc in a system of Tamaki's structured parts list because early prediction of manufacturing

behavior drives design changes which optimize the product's manufacturability and testability, thus improving product quality and reducing cost and utilizing a parts list would help facilitate this prediction. See column 6 of Tegethoff.

In reference to claim 72, Tamaki does not teach a compatibility prediction information output device configured to survey on predetermined items (i.e. packaging density, arrangement, and operation verification) based on parts information list created by parts information list creating/editing device and to create and output decision information for compatibility prediction based on results from said survey.

Tegethoff, however, teaches a method for manufacturing test simulation in electronic circuit design. Tegethoff teaches a test simulator that simulates a manufacturing text of boards and multichip modules from design concept to aid the designer in selecting trade-offs in design. The methods models fault probabilities for the circuit design based on the components. Tegethoff further discloses the Manufacturing Test Simulator (MTSIM) which is a concurrent engineering simulation tool for manufacturing test, that is, a tool to predict manufacturing test behavior while a product is still being designed. See column 6. MTSIM uses pareto analysis in which a user can evaluate simulation results to determine faults, test coverage, etc. Pareto analysis can be done at three levels of abstraction including individual components, groups of components with the same part number, and groups of components. All part numbers are assigned a category based on level of integration and functionality. See column 11. Furthermore, Tegethoff teaches that the technology of circuit board assembly is evolving

to support density demands of many modern circuit designs. Multi-chip modules and twelve-mil pitch surface mount technology (SMT) are frequently used to improve circuit density. SMT chip packages with lead counts of over 1000 are not uncommon. New fabrication processes are used to enable higher circuit densities usually have higher defect rates than older low density fabrication technologies. Tegethoff teaches identifying defects in packaging densities. See columns 1-4.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate Tegethoff's prediction concerning operation, simulation, etc in a system of Tamaki's structured parts list because early prediction of manufacturing behavior drives design changes which optimize the product's manufacturability and testability, thus improving product quality and reducing cost and utilizing a parts list would help facilitate this prediction. See column 6 of Tegethoff.

Claims 75-79 are rejected under the same rationale used in claims 67, 69, 70, 71, and 72 respectively above.

Claims 82-86 are rejected under the same rationale used in claims 67, 69, 70, 71, and 72 respectively above.

Claims 88-91 are rejected under the same rationale used in claims 67, 69, 70, and 71 respectively above.

Response to Arguments

6. Applicant's amendments and arguments filed on 12/20/07 have been fully considered. Applicant's amendments have been addressed in the claim rejections above.

On pages 13-16, Applicant argues none of the prior art teaches storing information about a plurality of electronic circuit boards including a listing of parts utilized for the electronic circuit boards. Examiner disagrees. Tamaki discloses that an electronic circuit board could be one of the products being created on a production line which meets the limitation, ***an electronic circuit board***. See page 10, paragraph [0155]. Tamaki discloses a unit for storing production plan information on how to produce a particular product such as an electronic circuit board along with a parts list storage section for storing the parts list information providing a list of required parts which meets the limitation, ***an assembly information storage configured to store assembly information for a plurality of electronic circuit boards, including a name of each electronic circuit board, and storing for each respective electronic circuit board a plurality of parts information including a name of parts utilized in said respective electronic circuit board***. See page 3, paragraph [0033], page 6, paragraph [0118], page 7, paragraph [0127]-[0128] and figures 1 and 3.

Applicant further argues none of the prior art teaches receiving an input indicating one of the electronic circuit boards and retrieving parts for the board. Examiner disagrees. See pages 1-2, paragraphs [0013], [0016], [0019], and [0021] which discuss a plurality of products in a production planning system. Tamaki discloses

a unit for storing production plan information on how to produce particular products along with a parts list storage section for storing the parts list information providing a list of required parts.

On page 15, Applicant argues Tamaki only teaches the electronic circuit board as a single part in an assembly line and is not directed to making an electronic circuit board. Examiner disagrees. Tamaki discloses that an electronic circuit board could be one of the products being created on a production line which meets the limitation, ***an electronic circuit board***. See page 10, paragraph [0155].

Applicant argues on page 16 of the Remarks that Tamaki is not directed to a system for creating or editing structured parts list information. Tamaki discloses a production planning system in which a production plan comprises a data storage unit for storing parts list information providing a list of required parts, a parts stock storage section indicating parts stock information which meets the preamble, ***a system for creating and/or editing structured parts***. See abstract and page 6, paragraphs [0117]-[0118].

Applicant further argues on pages 16-17 that Tamaki discloses a parts list storage section but does not disclose that the parts list storage section stores information of different assemblies such as an electronic circuit board including parts, and information of a name of the parts. Examiner disagrees that Tamaki does not disclose a plurality of products (i.e. assemblies, electronic circuit boards). See pages 1-2, paragraphs [0013], [0016], [0019], and [0021] which discuss a plurality of products in a production planning system. Tamaki discloses a unit for storing production plan

information on how to produce particular products along with a parts list storage section for storing the parts list information providing a list of required parts which meets the limitation, ***an assembly information storage configured to store assembly information for a plurality of assemblies including name of an assembly including a plurality of parts, and a plurality of parts information including name of parts utilized in said assembly.*** See page 3, paragraph [0033] , page 6, paragraph [0118], page 7, paragraph [0127]-[0128] and figures 1 and 3.

Examiner notes that a "product" is being interpreted as an "assembly". Furthermore, Examiner is interpreting "a list of parts information" as including the name of the parts used in the product. Tamaki further discloses a parts list storage section for storing the parts list information providing a list of required parts for a product. Applicant argues Tamaki does not teach "parts information retrieving device" or "assembly information update device". Tamaki discloses retrieving parts information from the production planning information and the parts list information stored in the data storage unit for use in a material resource planning unit which meets the limitation, ***a parts information retrieving device configured to retrieve a plurality of parts information from said assembly information storage based on input assembly information.*** Tamaki discloses an adjusting means in which superfluous or deficient parts are identified from the parts stock information and parts information. Superfluous parts are eliminated as are deficient parts and the production planning system is adjusted accordingly. See page 6, paragraph [0117]-[0122] and page 18. The parts list information is generated by the material resource plan unit for calculating the required

amount of material resources based on this list. The production system receives production planning information including parts list information from the parts acquisition system. See page 6. The updated structural parts list is provided to the production planning system where it is stored in a data storage unit which meets the limitation, ***an assembly information update device configured to replace the parts information corresponding to the assembly information with other parts information retrieved from the parts information storage, and to store the replaced parts information corresponding to the assembly information in a memory.*** See page 18, second column.

Applicant argues the parts list storage section of Tamaki does not store information on a plurality of assemblies. Examiner disagrees. See pages 1-2, paragraphs [0013], [0016], [0019], and [0021] which discuss a plurality of products in a production planning system.

On pages 18-19, Applicant argues Tamaki does not disclose the parts attribute information includes functions of parts. Tamaki does not expressly teach the “parts attribute information including functions of parts”; however, it was well known in the art at the time of the invention that any part of an assembly has a function. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention that a list of “required parts” would include the function of such parts because a “required part” would be identified by its use or function in the product especially when it is identified for use in an “assembly” or production line.

Regarding Applicant's arguments directed to the motivation of combining Tegethoff and Tamaki, Examiner disagrees. As stated in the rejections above, it would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate Tegethoff's prediction concerning operation, simulation, etc in a system of Tamaki's structured parts list because early prediction of manufacturing behavior drives design changes which optimize the product's manufacturability and testability, thus improving product quality and reducing cost and utilizing a parts list would help facilitate this prediction. See column 6 of Tegethoff.

Applicant argues there is no basis for the combination because Tegethoff's simulation of an electronic circuit design is irrelevant to the system of Tamaki. Examiner disagrees. It has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Tegethoff is concerned method for manufacturing test simulation in electronic circuit design. Tegethoff teaches a test simulator that simulates a manufacturing text of boards and multichip modules from design concept to aid the designer in selecting trade-offs in design. The methods models fault probabilities for the circuit design based on the components. Tegethoff further discloses the Manufacturing Test Simulator (MTSIM) which is a concurrent engineering simulation tool for manufacturing test, that is, a tool to predict manufacturing test behavior while a product is still being designed. See column 6.

MTSIM uses pareto analysis in which a user can evaluate simulation results to determine faults, test coverage, etc. Pareto analysis can be done at three levels of abstraction including individual components, groups of components with the same part number, and groups of components. All part numbers are assigned a category based on level of integration and functionality. See column 11. Furthermore, Tegethoff teaches that the technology of circuit board assembly is evolving to support density demands of many modern circuit designs. Multi-chip modules and twelve-mil pitch surface mount technology (SMT) are frequently used to improve circuit density. SMT chip packages with lead counts of over 1000 are not uncommon. New fabrication processes are used to enable higher circuit densities usually have higher defect rates than older low density fabrication technologies. Tegethoff teaches identifying defects in packaging densities. See columns 1-4.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate Tegethoff's prediction concerning operation, simulation, etc in a system of Tamaki's structured parts list because early prediction of manufacturing behavior drives design changes which optimize the product's manufacturability and testability, thus improving product quality and reducing cost and utilizing a parts list would help facilitate this prediction. See column 6 of Tegethoff.

In view of comments above, the rejection is maintained.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rachna Singh whose telephone number is 571-272-4099. The examiner can normally be reached on M-F (8:30AM-6:00PM). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doug Hutton can be reached on 571-272-4137.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Rachna Singh/
Rachna Singh
Primary Examiner, Art Unit 2176